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(PTO ASSISTANCE)

Application : 10/673,092 Examiner : A.G. Ghyka GAU : 2812

From: S. Winslow Location: IDC FMF FDC Date: 12-27-05

Tracking #: EPM 10/673,092 Week Date: 10-3-05

DOC CODE	DOC DATE	MISCELLANEOUS
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<input type="checkbox"/> OATH	_____	
<input type="checkbox"/> 312	_____	
<input checked="" type="checkbox"/> SPEC	<u>9-25-03</u>	

[RUSH] MESSAGE: Page 6 of specification, paragraph 0022,
missing serial numbers.

please advise

Thanks

[XRUSH] RESPONSE: _____

See misc comm

Don

INITIALS: EW

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REV 10/04

OFFICIAL COMMUNICATION**Certificate of Transmision under 37 CFR 1.8**

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Examiner:	Rori Burch
Technology Center:	Publishing Division
Fax No.:	(571) 273-9009
USSN:	10/673092
Filed:	September 25, 2003
Inventor(s):	Dubrow
Title:	Methods, Devices and Compositions for Depositing and Orienting Nanostructures
Document(s):	Transmittal Amendment After Final Copy of Notice

Total Number of Pages, including Certificate: **6**

Michelle Chan
Signature

Michelle Chan
Typed or printed name of person signing Certificate

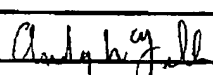
PTO/SB/21 (09-04)

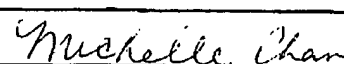
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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/873,0082
	Filing Date	September 25, 2003
	First Named Inventor	Dubrow
	Art Unit	2812
	Examiner Name	Ghyka
Total Number of Pages in This Submission	Attorney Docket Number	01-003600

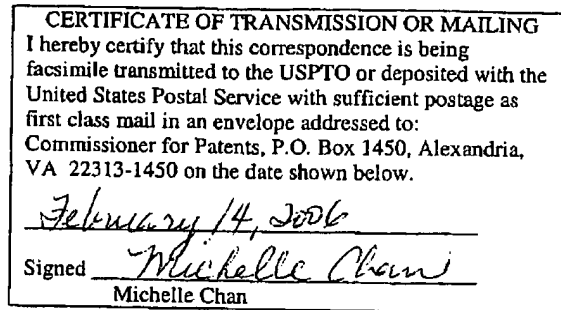
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Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	Nanosys, Inc.		
Signature			
Printed name	Andrew L. Filler		
Date	2-14-06	Reg. No.	44,107

CERTIFICATE OF TRANSMISSION/MAILING			
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.			
Signature			
Typed or printed name	Michelle Chan	Date	February 14, 2006

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Appl. No. : 10/673,092 Confirmation No. 7555
Applicant : Robert Dubrow et al.
Filed : September 25, 2003
TC/A.U. : 2812
Examiner : Ghyka
Docket No. : 01-003600
Customer No. : 33140

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER ALLOWANCE

Sir:

In response to the Communication of February 6, 2006, please amend the
above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.

Appl. No. 10/673,092
Amnd dated February 14, 2006
Reply to Office Action of February 6, 2006

Amendments to the Specification:

Please replace paragraph [0022] with the following amended paragraph:

[0022] In a modified application of the nanowire electronics shown in Figure 2, large numbers of nanowires can be used, e.g., as a film, to provide electronics with enhanced properties, such as ease of fabrication of large area electronics, e.g., as illustrated in transistor array 300, and relatively high performance. In particular, as can be seen in panel A, a large area macroelectronic device, array or substrate, e.g., array 300, is produced using populations of nanowires disposed over the surface of the substrate or portions thereof. In this array, individual devices, e.g., transistor 302, can further take advantage of the high aspect ratio of these nanowire materials by including large numbers of oriented wires that substantially span the space between two or more electrodes. In particular, Panel B illustrates a simplified electronic circuit device from array 300, using large numbers of oriented nanowires 304 deposited upon a substrate surface 306 as the semiconductive channel between two electrodes, e.g., source electrode 308 and drain electrode 310. By so orienting these materials, one can effectively provide single crystal semiconductor electron mobilities between the electrodes, e.g., in individual wires, while providing sufficient current density (e.g., through multiple wires) with extremely low lateral electron mobilities, e.g. orthogonal to the direction from one electrode to another. Further, as noted above, the overall small scale of the individual nanowires in both length and width dimensions, allows for production of flexible overall electronic devices using simplified processing technologies. As shown, the transistor 302 also includes gate electrode 312. Fabrication, application and performance of devices like that schematically illustrated in panel B of Figure 3 are described in substantial detail in, e.g., U.S. Patent Application No. 60/414,323 and 60/414,359, each filed September 30, 2002, 60/468,276, filed May 7, 2003, ~~_____ (Attorney Docket No. 01-001700)~~ 60/493,005, filed August 7, 2003, 60/445,421 filed February 5, 2003, 60/474,065, filed May 29, 2003 and ~~_____ (Attorney Docket No. 01-002900)~~ 60/488,801, filed July 22, 2003, the full disclosures of which are hereby incorporated herein in their entirety for all purposes.

Appl. No. 10/673,092
Amnd dated February 14, 2006
Reply to Office Action of February 6, 2006

Remarks

Applicant has updated the specification to include provisional serial numbers which were missing in the original specification as requested in the communication. No new matter is being introduced.

Respectfully submitted,



Andrew L. Filler
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**UNITED STATES PATENT AND TRADEMARK OFFICE**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Serial Number
10673092

Date Mailed
2/06/06

NOTICE TO FILE CORRECTED APPLICATION PAPERS***Notice of Allowance Mailed***

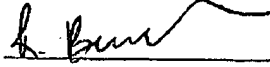
This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given 30 days from the mail date of this Notice within which to correct the informalities indicated below. A failure to reply will result in the application being ABANDONED. This period for reply is NOT extendable under 37 CFR 1.136 (a) or (b).

- ◆ Specification page 6, serial numbers are missing. Fax missing information to number below or e-mail.
- For status updates visit <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR System, contact the Electronic Business Center (EBC) toll free at 866-217-9197.

APPLICANT MUST SUPPLY MISSING INFORMATION WITHIN 30 DAYS OF THE MAIL DATE OF THIS NOTICE.

A copy of this notice MUST be returned with the reply. Please address response to Commissioner for Patents P.O. Box 1450
Alexandria, VA 22313-1450



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